# PLX Technology

## The Leading Supplier of PCI Express and Standard I/O Interconnect Silicon

**PRODUCT GUIDE**
**VERSION 4.0, 2006**

PLX Technology, Inc. is the leading supplier of PCI Express and standard I/O interconnect silicon to the communications, server, storage, embedded-control, and consumer industries. With an ever increasing number of I/O and bus standards in the marketplace, PLX provides solutions to bridge, isolate, expand, and switch.

We support a vast array of standards including PCI Express*, PCI, PCI-X, USB 2.0 as well as local or generic buses.

The PLX solution includes a complete combination of high-performance silicon, hardware and software design tools, supported by partnerships throughout the industry.

These innovative solutions are designed to enable our customers to develop systems with legacy and industry-leading, cutting-edge products.

PLX has been developing I/O interconnect products since 1986.

PLX is publicly traded (NASDAQ: PLXT) and headquartered in Sunnyvale, CA, USA. PLX's European operations are based in the United Kingdom; its Asian operations in China and Japan.

PLX TECHNOLOGY®
THE I/O INTERCONNECT SOLUTION

www.plxtech.com

# PEX 8111

## *PCI Express-to-PCI Bridge*

### *The World's Smallest PCI Express Bridge*

The PLX Technology ExpressLane PEX 8111 is a high performance bridge that enables designers to migrate legacy PCI bus interfaces to the advanced serial, PCI Express architecture.

The **tiny BGA package** and **low power** consumption make it the ideal bridge for applications with limited board space and power budget.

The PEX 8111 is equipped with an **integrated PCI Express PHY** that provides a x1 link at 2.5 Gbps. Supporting standard PCI Express signaling compliant to the 1.0a specification, the integrated PHY delivers high bandwidth at a low pin count (4-pins) using LVDS technology.

The single parallel bus segment supports the latest PCI bus protocol. With a 32-bit wide parallel data path running at 66MHz, the standard PCI interface accommodates a broad range of legacy applications.

### *Forward and Reverse Bridging*

The PEX 8111 can be configured to support either **forward** or **reverse** bridging operation as defined by the PCI Express to PCI/PCI-X Bridge Specification 1.0. As a reverse bridge, the PEX 8111 allows conventional PCI CPU subsystems to configure and control downstream PCI Express devices. This feature facilitates the bridging of high performance PCI Express native silicon into legacy PCI systems. The PEX 8111 includes provisions for reverse bridging such as reverse configuration and interrupt handling.

| Interfaces | Description |
|---|---|
| PCI Express Link Width | Single link of x1 |
| PCI Express Lane Speed | 2.5 Gbps TX and RX lanes |
| PCI Express Port | R1.0a compliant, polarity reversal |
| PCI Bus Type | PCI r3.0, 32-bit, 66MHz |
| **Electrical Characteristics** | **Description** |
| Core Voltage | 1.5V |
| SerDes reference | 1.5V |
| PCI I/O | 3.3V (5V tolerant) |
| **Packaging** | **Description** |
| Package Type* | 144-ball, Plastic BGA<br>161-ball, fine-pitch, Plastic BGA |
| Package Size | 13mm x 13mm<br>10mm x 10mm (fine-pitch) |
| Operating Temperature Range | Commercial Grade 0° to +70° C |
| Power Dissipation | 0.4W Maximum |
| **Features** | **Description** |
| Bridge Modes | Forward and Reverse |
| PCI Arbitration | Up to four (4) external master devices |
| JTAG | Yes |
| EEPROM | Yes |
| GPIO | Four (4) |
| Rapid Development Kits | PEX 8111RDK-F Forward Mode RDK<br>PEX 8111RDK-R Reverse Mode RDK |
| Shared RAM | Internal 8kbyte |

* Available in standard and lead-free packaging. See complete list of part numbers on our website at http://www.plxtech.com/products/leadfree.asp

# PEX 8114

## *PCI Express to PCI/PCI-X Bridge*

### *The most flexible, high performance PCI Express Bridge*

The PLX Technology ExpressLane PEX 8114 is a high performance bridge that enables designers to migrate legacy PCI and PCI-X bus interfaces to the advanced serial PCI Express architecture.

This two(2) port device is equipped with a standard, but flexible **PCI Express PHY** that scales to provide up to one Gigabyte per second of maximum throughput per transmit and receive direction.

The single parallel bus segment supports the advanced PCI-X protocol. With a 64-bit wide parallel data path running at 133MHz, the standard PCI-X interface can reach a matching bandwidth of one Gigabyte per second. For legacy PCI applications, the bus segment also supports conventional PCI bus protocols.

### *Forward and Reverse Bridging*

The PEX 8114 can be configured to support either **forward** or **reverse** bridging operation as defined by the PCI Express to PCI/PCI-X Bridge Specification 1.0. As a reverse bridge, the PEX 8114 allows conventional PCI/PCI-X CPU subsystems to configure and control downstream PCI Express devices. This feature facilitates the bridging of high performance PCI Express native silicon into legacy PCI systems. The PEX 8114 includes provisions for reverse bridging such as reverse configuration, root functions, interrupt handling, and advanced error reporting.

### *Non-Transparent Bridging*

The PEX 8114 can also be configured as a **non-transparent bridge**, allowing distinct processor and memory domains to exist on both primary and secondary sides of the device. Non-Transparent Bridging can be used for **intelligent adapter designs** as well as in **dual or multi-host environments**.

| Interfaces | Description |
|---|---|
| PCI Express Link Width | Single link of x4, x2 or x1 |
| PCI Express Lane Speed | 2.5 Gbps TX and RX lanes |
| PCI Express Port | R1.0a compliant, lane reversal, polarity reversal |
| PCI/PCI-X Bus Type | PCI-X, 64-bit, 133-, 100-, 66 MHz<br>PCI, 64-bit, 66/50/33/25 MHz PCI r2.3 |
| **Electrical Characteristics** | **Description** |
| Core Voltage | 1.0V |
| SerDes reference | 1.5V |
| PCI/PCI-X I/O | 3.3V |
| **Packaging** | **Description** |
| Package Type * | 256-ball, Plastic BGA |
| Package Size | 17mm x 17mm |
| Operating Temperature Range | Industrial Grade -40° to +85° C |
| Power Dissipation | 2W Maximum, no heat sink |
| **Features** | **Description** |
| Bridge Modes | Forward and Reverse |
| Transparency Modes | Forward Transparent, Forward Non-Transparent and Reverse Transparent |
| PCI/PCI-X Arbitration | Up to four(4) external master devices |
| JTAG | Yes - 1149.1/1149.6 |
| EEPROM | Yes |
| Secondary PCI/PCI-X Clock Outputs | Four (4) |
| Rapid Development Kits | PEX 8114RDK-F Forward Mode RDK<br>PEX 8114RDK-R Reverse Mode RDK |

* Available in standard and lead-free packaging. See complete list of part numbers on our website at http://www.plxtech.com/products/leadfree.asp

# PEX 8311

## *ExpressLane - PCI Express to Generic Local Bus Bridge*

The multi-purpose and feature rich PCI Express Bridge offers generic local bus to PCI Express (PCIe) bridging capability enabling users to add scalable high bandwidth interconnection to a wide variety of applications. Many embedded system designs utilizing PCI today can easily migrate to PCIe. The bridge offloads the computational tasks associated with transferring data between a generic local bus and a PCIe port.

### *Complete Conversion from PCI Express Signaling*

The PEX 8311 provides complete local bus to PCIe translation. Full PCIe packet generation and decoding combined with local/PCIe address translation, MSI interrupt handling, and WAKE#/Beacon signals are supported.

### *Highly Flexible Generic Local Bus*

The PEX 8311 offers a highly flexible yet low overhead "generic" local bus which provides a direct connection to two generic industry-standard interconnect buses. The bus protocol can be set to the non-multiplexed address and data "C-Mode" or multiplexed address/data "J-Mode". This bus can be directly connected to many processors with minimal or no glue logic. Up to six loads including memory, FPGAs, FIFOs and other devices can be simultaneously placed on this bus. With its 32-bit, 66MHz operation, the local bus can transfer zero wait state bursts up to 264MB/sec.

### *Dual Independent Full Feature DMA Channels*

The PEX 8311 provides two data transfer channels with support for block, scatter-gather, ring management, and demand modes. These channels provide independent data transfers with the bridge initiating both the PCIe and local bus. Deep FIFO buffers and read ahead with programmable read pre-fetch counters optimize throughput.

### *Root Complex and EndPoint Modes*

The PEX 8311 bridge supports both Root Complex and EndPoint modes of operation. This flexibility allows a Root Complex system designer to utilize the part as a type of "north bridge" whereby multiple Local Bus components present including a processor, memory, DSP, etc., can communicate with each other as well with downstream PCIe devices.

| Interfaces | Description |
|---|---|
| PCI Express Lane/Local Bus | 1 lane to 8/16/32-bit 66 MHz Local Bus Bridge |
| PCI Express Lane Speed | 2.5 Gbps per lane |
| PCI Express Port | R1.0a Compliant, polarity reversal |
| **Electrical Characteristics** | **Description** |
| Core Voltage | 1.5V and 2.5V |
| SerDes reference | 1.5V |
| Hot Plug & I/O | 3.3V/5V Tolerant |
| **Packaging** | **Description** |
| Package Type * | 337-pin, plastic BGA |
| Package Size | 21mm x 21mm |
| Operating Temperature Range | 0°C to +70° C |
| Power Dissipation | 1.0W, no airflow or heat sink required |
| **Features** | |
| EEPROM | Yes |
| I20 Messaging Unit | Yes |
| General Purpose I/O pins | Yes-Four plus 1 GPI, 1 GPO |
| **Development Tools** | **Description** |
| PEX 8311RDK | Hardware, SW drivers, API, GUI and design guide |

***** Available in standard and lead-free packaging. See complete list of part numbers on our website at http://www.plxtech.com/products/leadfree.asp

# PEX 8548, PEX 8532, PEX 8524, and PEX 8516

## *Versatile PCI Express Switches*

PLX Technology ExpressLane switch consists of high performance, multipurpose, highly configurable devices compliant with the PCI Express Base specification. These switches can be used in wide variety of applications such as **fan-out, aggregation**, **peer-to-peer**, **fabric backplane,** and **intelligent I/O** module applications.

### *Flexible Port Configurations*

The ExpressLane Switches offer highly configurable ports. For example, with the PEX 8532, in a fan-out application one may configure the upstream port as x8 and the downstream ports as six x4 ports; two x8 and two x4 ports; three x8 ports; or any other combination that does not exceed the maximum number of lanes or ports. For a peer-to-peer application, all eight ports can be configured as x4. In a port aggregation application, four x2 or x4 ports can be aggregated into one x8 or x16 port.

### *Quality of Service*

The ExpressLane Switch family provides end-to-end CRC protection (ECRC) and Poison-bit support to enable designs that require guaranteed error-free packets. These features are optional in the PCI Express specification, but PLX provides them across our entire PCI Express product line. The PEX 8532, 8524 and 8516 offer two full-featured Virtual Channels (VCs). In addition, these devices offer user-selectable Virtual Channel arbitration algorithms to enable fine tuning of the Quality of Service (QoS) required for a specific application.

### *Non-Transparent Bridging*

The PEX 8532, 8524 and 8516 support full Non-Transparent Bridging functionality to allow implementation of multi-host systems and intelligent I/O modules in communications, storage, & blade server applications.

### *Low Power with Granular SerDes Control*

All ExpressLane Switches provide low power capability that is fully compliant with the PCI Express power management specification. In addition, the SerDes physical links can be configured for low, typical, or high power, or turned off when unused for even lower power.

### *Hot Plug for High Availability*

Each downstream port of the ExpressLane switches (excluding the PEX 8548 which supports 3 total) includes a Standard Hot Plug Controller that acts as a master to manage Hot-Plug events. The upstream port is a fully compliant Hot Plug client, allowing it to be used on hot-pluggable adapter cards, backplanes and fabric modules.

| **Interfaces** | |
|---|---|
| PCI Express Lane/Port count | PEX 8548: 48 lanes with 9 configurable ports<br>PEX 8532: 32 lanes with 8 configurable ports<br>PEX 8524: 24 lanes with 6 configurable ports<br>PEX 8516: 16 lanes with 4 configurable ports |
| PCI Express Lane Speed | 2.5 Gbps per lane (per LVDS pair) |
| PCI Express Lanes | Lane / Polarity reversal & lane status pins |
| **Electrical Characteristics** | |
| Core Voltage | 1.0V |
| SerDes reference | 1.5V |
| Hot-plug & I/O | 3.3V |
| **PEX 8548** | |
| Package Type* | 736-ball, Plastic BGA |
| Package Size | 37.5mm x 37.5mm |
| Operating Temperature Range | -40° to +85°C |
| **PEX 8532** | |
| Package Type * | 680-ball, Plastic BGA |
| Package Size | 35mm x 35mm |
| Operating Temperature Range | -40° to +85° C |
| **PEX 8524** | |
| Package Type * | 644-ball Plastic BGA |
| Package Size | 31mm x 31mm |
| Operating Temperature Range | -40° to +85° C |
| **PEX 8516** | |
| Package Type * | 312-ball, Plastic BGA |
| Package Size | 27mm x 27mm |
| Operating Temperature Range | -40° to +85° C |
| **Development Tools** | |
| PEX 8548RDK<br>PEX 8532RDK<br>PEX 8524RDK<br>PEX 8516RDK | Available with x16, x8, x4 Connectors<br>Available with x16, x8, x4, x1 Connectors<br>Available with x16, x8, x4, x1 Connectors<br>Available with x4, x1 Connectors |

* Available in standard and lead-free packaging. See complete list of part numbers on our website at http://www.plxtech.com/products/leadfree.asp

# PEX 8508, 8517 and 8518

## *Economical Low Latency PCI Express Switches*

The PLX Technology ExpressLane PEX 8508, 8517 and 8518 are high performance, low latency, multipurpose, and highly flexible switches compliant to the recently released PCI Express specification r1.1. The PEX 8508, 8517 and 8518 devices can be used as fan-out, aggregation, or peer-to-peer switches in a wide variety of cost-sensitive mass market applications ranging from office automation and laptop docking stations to network interface adapters. The PEX 8508 is a perfect fit when used for processor isolation applications in redundant/fail-over boards for servers and storage systems. Operation and port width assignments can be configured through upstream software, an $I^2C$ interface, or optional EEPROM.

### *Flexible Port Configuration*

The PEX 8508, 8517 and 8518 switches offer up to five ports each. All three switches can be configured to any legal combination of lanes per port for fan-out, data aggregation, and peer-to-peer switching as long as user does not exceed the devices port per lane limit.

### *Low Latency and High Performance*

The PEX 8508, 8517 and 8518 switches have a cut-through based architecture allowing ingress/egress latency through the switches, under 150ns. Both switches have a fully non-blocking architecture.

### *End-to-end Packet Integrity*

The PEX 8508, 8517 and 8518 provide end-to-end CRC protection (ECRC) and Poison bit support to enable designs that require guaranteed error-free packets. These features are optional in the PCI Express specification, but PLX provides them across its entire PCI Express product line.

### *Non-Transparent Bridging*

The PEX 8508, 8517 and 8518 support full non-transparent bridging functionality to allow implementation of multi-host systems and intelligent I/O modules in applications such as communications, storage, and blade servers. The port chosen to be non-transparent is fully selectable.

### *Two Virtual Channels*

The PEX 8508 supports up to 2 full-featured Virtual Channels (VCs) and full 8 Traffic Classes (TCs). In addition, the device offers user-selectable Virtual Channel arbitration algorithms to enable fine tuning of the Quality of Service (QoS) required for a specific application.

### *Low Power with Granular SerDes Control*

The PEX 8508, 8517 and 8518 provide low power capability that is fully compliant with the PCI Express power management specification. In addition, the SerDes physical links can be configured for low, typical or high power or turned off when unused for even lower power. Vaux, Wake#, and Beacon are supported and allow $D^3$ (cold) device state support for further power savings.

### *Hot Plug for High Availability*

Each downstream port of the PEX 8508, 8517 and 8518 includes a Standard Hot Plug Controller that acts as a master to manage I/O module Hot-Plug events. The upstream port is a fully compliant hot-plug client, allowing it to be used on hot-pluggable adapter cards, backplanes and fabric modules.

| Interfaces | Description |
|---|---|
| PCI Express Lane/Port Count | PEX 8508: 8 lanes with 5 configurable ports<br>PEX 8517: 16 lanes with 5 configurable ports<br>PEX 8518: 16 lanes with 5 configurable ports |
| PCI Express Lane Speed | 2.5 Gbps per lane (per LVDS pair) |
| PCI Express Port | r1.1 Compliant, lane reversal, polarity reversal, and lane status pins |
| **Electrical Characteristics** | **Description** |
| Core Voltage | 1.0V |
| SerDes Reference | 1.5V |
| Hot Plug & I/O | 3.3V |
| **PEX 8518** | **Description** |
| Package Type * | 376-ball, Plastic BGA (standard and lead-free) |
| Package Size | 23mm x 23mm |
| Operating Temperature Range | -40° to 85°C |
| Power Dissipation | 3.0W, no airflow or heat sink required |
| **PEX 8517** | **Description** |
| Package Type * | 312-ball, Plastic BGA |
| Package Size | 27mm x 27mm |
| Operating Temperature Range | -40° to 85°C |
| **PEX 8508** | **Description** |
| Package Type * | 296-pin, plastic BGA |
| Package Size | 19mm x 19mm |
| Operating Temperature Range | -40° to 85°C |
| Power Dissipation | 2.5W, no airflow or heat sink required |
| **Development Tools** | **Description** |
| PEX 8518RDK | Hardware, SW drivers, API, GUI and design |
| PEX 8508RDK | Hardware, SW drivers, API, GUI and design |

* Available in standard and lead-free packaging. See complete list of part numbers on our website at http://www.plxtech.com/products/leadfree.asp

# NET 2272, NET 2280, and NET 2282

## *Hi-Speed USB 2.0 Peripheral Controllers*

PLX Technology offers a complete line of USB 2.0 peripheral controller solutions. Our products emphasize superior performance, strict compliance to industry standards, and dramatic power savings. These controllers feature diverse, programmable interfaces to gluelessly connect to various applications. Our PCI-based reference design kits offer easy PC-based development with many application, driver, and firmware examples, supporting Windows, Linux, VxWorks, and WinCE. PLX's USB products are used extensively in printers, portable media players, GPS navigation systems, Notebook and Ultra Mobile PCs, TV tuners, WLAN devices, mobile phones, and digital camcorders.

NetChip USB Technology

HI-SPEED CERTIFIED USB

### NET 2272

Local Bus to Hi-Speed USB 2.0 Peripheral Controller

- Low power and small packaging make it ideal for bus or battery-powered devices
- Fastest sustained transfer rate, up to 40MBytes/sec
- Flexible I/O voltage range from 1.8V to 5V
- Low power process (186mW active, 8.1µW standby)
- Smallest packaging (6x6mm BGA package)
- Dynamic Virtual Endpoint Technology™ actualizes 30 independent USB endpoints
- Configurable CPU interface
- WinXP, Vista, Linux, and WinCE support

### NET 2280

PCI to Hi-Speed USB 2.0 Controller

- PCI 33MHz / 32-bit interface
- Instantly add a Hi-Speed USB 2.0 peripheral port into any PCI-based systems
- USB Duet Technology, add Hi-Speed USB 2.0 peripheral functionality to laptop PCs and Ultra Mobile PCs
- Ideal for PCI embedded systems like printers and test instruments
- 4 DMA controllers with Scatter Gather descriptor capability
- USB Auto-Enumeration
- Firmware available to support many standard USB Classes (Printer, Mass Storage, MTP, Video, Audio, etc.)
- WinXP, Vista, Linux, and WinCE support

### NET 2282

PCI to Hi-Speed USB 2.0 Peripheral Bridge

- Optimized for converting PCI adapters to USB 2.0 devices
- PCI 66MHz/32-bit interface
- PCI Host capability for initializ ing and configuring the existing PCI chip
- Integrated PCI arbiter to support mastering PCI devices
- Integrated 8051 CPU @ 30MHz
- 32K of Shared RAM for emulat ing main system memory
- WinXP, Vista, Linux, and WinCE support

# NET 2272, NET 2280, and NET 2282

## *Hi-Speed USB 2.0 Peripheral Controllers Overview*

| | NET2272 | NET2280 | NET2282 |
|---|---|---|---|
| CPU Interface | Configurable 8/16 bit asynchronous local bus | PCI v3.0 compliant 33MHz / 32 Bits | PCI v3.0 compliant 66MHz / 32 Bits |
| Sustained Performance | Up to 40MBytes/sec | Up to 40MBytes/sec | Up to 40MBytes/sec |
| Active Power | 186mW | 260mW | 220.2mW |
| Suspended Power | 8.1µW | 0.25µW | 316µW |
| I/O Voltage | 1.8V to 5V | 3.3V or 5V | 3.3V or 5V |
| Package* | 10mm x 10mm 64-Pin TQFP<br>6mm x 6mm 64-Ball BGA | 14mm x 14mm 120-Pin TQFP<br>8mm x 8mm 121-Ball FPBGA | 14mm x 14mm 120-Pin QFP |
| Applications | Portable media players, GPS systems, mobile phones, PDAs, digital camcorders | USB Duet Port, Notebook PCs, Ultra Mobile PCs, printers, test equipment and other PCI-embedded systems | Convert PCI adapters like TV tuners, video capture cards, and wireless LAN adapters to USB 2.0 devices |
| Development Kits | NET 2272 RDK-II | NET 2280 EVB<br>NET 2280 EVB-SW | NET 2282 RDK |

* Available in lead-free packaging. See complete list of part numbers on our website at http://www.plxtech.com/products/leadfree.asp

**Development Environment and Support**

| Hardware | Software |
|---|---|
| ■ PCI adapter card form factor plugs directly into a PC for Windows, Linux, and WinCE based development<br>■ Converts any standard PC into a USB 2.0 device or development station<br>■ Develop your software on proven hardware before your platform is ready<br>■ Schematics, BOM, and Gerber files<br>■ Schematic and layout review | ■ Remote PCI (RPCI) simplifies PCI to USB conversion<br>■ Windows, Linux, VxWorks and WinCE Support<br>■ API abstracts hardware elements<br>■ Standard USB Class device support (Printer, Mass Storage, Communications Devices, Video, Audio, MTP, R-NDIS)<br>■ Reference firmware with source code<br>■ USB host-side drivers with source code<br>■ Host-side applications for test and debug engineering |

# PLX FastLane™ PCI and PCI-X Bridges

***Get in the FastLane with the PCI 6000 Series***

The PLX FastLane PCI 6000 series has the industry's broadest set of PCI-to-PCI bridges. These bridges allow more devices to be attached to the PCI bus, and provide the ability to include intelligent adapters on a PCI bus. In addition, these bridges allow PCI buses of different speeds to be part of the same subsystem.

The PLX FastLane PCI and PCI-X family of interconnect devices include PCI-to-PCI and PCI-X to PCI-X bridging devices, offering system designers several distinct features along with vastly improved I/O performance. The PLX FastLane PCI 6000 series of PCI-to-PCI bridging products provides designers with support for the entire range of current PCI bus widths and speeds, including 32-bit, 33MHz; 64-bit, 66MHz; and the latest 64-bit, 133MHz PCI-X variety of the standard.

The FastLane PCI 6000 product line is distinguished by featuring the lowest power, highest performance and smallest footprints in the industry. The line includes features such as the ability to clock the PCI bus segments asynchronously to one another and to operate the parts in either transparent or true non-transparent mode. This is crucial when the same module is designed to be used as a host or a peripheral in a system. In addition, all PLX FastLane PCI 6000 series bridges are 5V-tolerant.

These products were designed to provide high-performance interconnect for servers, storage, telecommunications, networking, and embedded applications. Like all PLX interconnect chips, the PCI 6000 series products are supported by PLX's comprehensive reference design tools and the industry-recognized PLX support infrastructure.

***P-to-P Bridge Rapid Development Kits (RDK)***

The PLX FastLane PCI 6000RDK series includes PCI 6000 series devices on evaluation boards along with documentation to facilitate rapid development of systems using PLX FastLane PCI 6000 series PCI-to-PCI bridges.

# Table 1. FastLane PCI and PCI-X Bridges

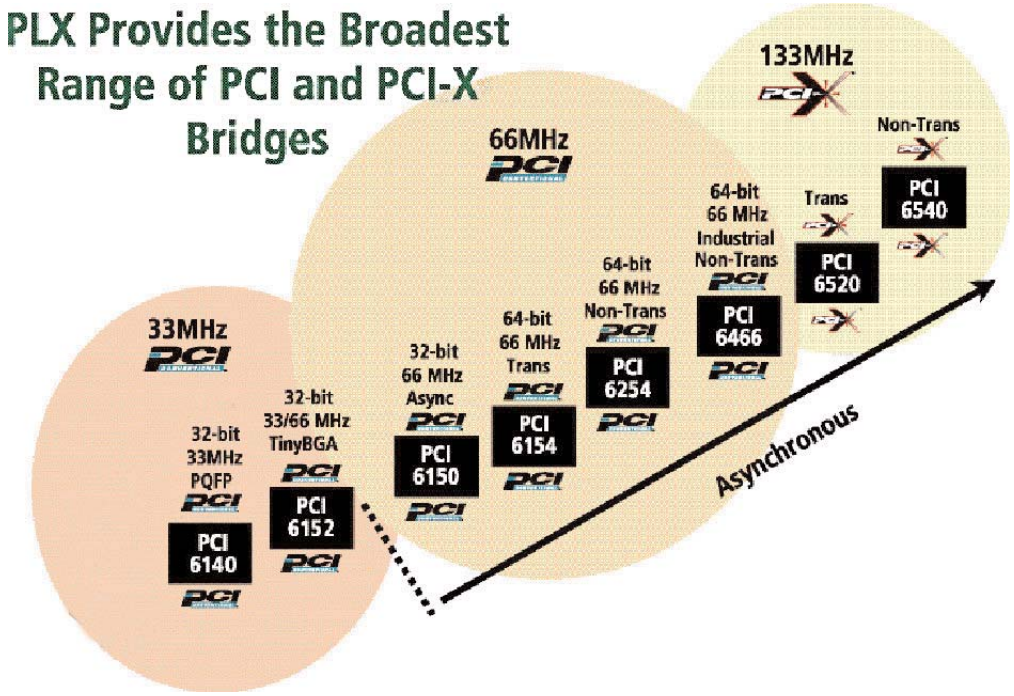
| | PCI 6140-AA33PC<br>PCI 6140-AA33PC G | PCI 6150-BB66BC<br>PCI 6150-BB66PC<br>PCI 6150-BB66BC G<br>PCI 6150-BB66PC G | PCI 6152-CC33BC<br>PCI 6152-CC33PC<br>PCI 6152-CC33BC F<br>PCI 6152-CC33PC G | PCI 6152-CC66BC<br>PCI 6152-CC66BC F | PCI 6154-BB66BC<br>PCI 6154-BB66BC G | PCI 6254-BB66BC<br>PCI 6254-BB66BC G | PCI 6466-CB66BI<br>PCI 6466-CB66BI G | PCI 6520-CB13BI<br>PCI 6520-CB13BI G | PCI 6540-CB13BI<br>PCI 6540-CB13BI G |
|---|---|---|---|---|---|---|---|---|---|
| PCI Bus Type | 32-bit 33MHz PCI | 32-bit 66MHz PCI | 32-bit 66MHz PCI | 32-bit 66MHz PCI | 64-bit 66MHz PCI | 64-bit 66MHz PCI | 64-bit 66MHz PCI | 64-bit 133MHz PCI-X | 64-bit 133MHz PCI-X |
| PCI Local Bus Support | Rev. 2.1 compliant | Rev. 3.0 compliant | Rev. 2.2 compliant | Rev. 2.2 compliant | Rev. 3.0 compliant | Rev. 3.0 compliant | Rev. 3.0 compliant | Rev. 3.0 compliant | Rev. 3.0 compliant |
| 3.3V and 5V Tolerant I/O | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Asynchronous Operation | No | 25MHz to 66MHz | No | No | 25MHz to 66MHz | 25MHz to 66MHz | 25MHz to 66MHz | 25MHz to 133MHz | 25MHz to 133MHz |
| Power Dissipation | 200mW | 1.8W | 300mW | 300mW | 2.0W | 2.0W | 1.0W | 2.4W | 3.0W |
| GPIO Interface | No | Four GPIO Pins | Four GPIO Pins | Four GPIO Pins | Four GPIO Pins | 16 GPIO Pins | 16 GPIO Pins | 8 GPIO Pins | 16 GPIO Pins |
| Transparency Modes | Transparent only | Transparent only | Transparent only | Transparent only | Transparent only | Transparent, Non-transparent and Universal modes | Transparent, Non-transparent and Universal modes | Transparent only | Transparent, Non-transparent and Universal modes |
| CompactPCI Compatible Hot Swap | Friendly | Rev 2.0 with PI=1 | Friendly | Friendly | No support | Rev 2.0 with PI=1 | Rev 2.0 with PI=1 | No support | Rev 2.0 with PI=1 |
| Data FIFO | No | 1KB FIFO | No | No | 1KB FIFO | 1KB FIFO | 10KB FIFO | 10KB FIFO | 10KB FIFO |
| # of Bus Masters on Secondary Bus | Up to 4 | Up to 9 | Up to 4 | Up to 4 | Up to 9 | Up to 9 | Up to 8 | Up to 8 | Up to 8 |
| Retry Architecture | Standard | Standard | Performance Optimized | Performance Optimized | Standard | Standard | Standard | Standard | Standard |
| Programmable Flow-Thru | No | Yes | No | No | Yes | Yes | Yes | Yes | Yes |
| Programmable Prefetch | No | Up to 4KB | No | No | Up to 4KB | Up to 4KB | Up to 4KB | Up to 2KB | Up to 2KB |
| Zero wait state burst | Up to 1KB | Up to 1KB | Up to 4KB | Up to 4KB | Up to 4KB | Up to 4KB | Up to 4KB | Up to 4KB | Up to 4KB |
| EEPROM support | No | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Vital Product Data Registers | No | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| D3 Wakeup Power Mgmt | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Secondary Clock Outputs | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| JTAG Support | No | IEEE 1149.1 compliant | No | No | IEEE 1149.1 compliant | IEEE 1149.1 compliant | IEEE 1149.1 compliant | IEEE 1149.1 compliant | IEEE 1149.1 compliant |
| Packaging * | PQFP-128 | BGA-256<br>PQFP-208 | Tiny BGA-160<br>PQFP-160 | Tiny BGA-160 | PBGA-304 | PBGA-365 | PBGA-380 | PBGA-380 | PBGA-380 |
| Package Size | 23mm x 17mm | 17mm x 17mm<br>31mm x 31mm | 15mm x 15mm<br>32mm x 32mm | 15mm x 15mm<br>No PQFP | 31mm x 31mm | 31mm x 31mm | 27mm x 27mm | 27mm x 27mm | 27mm x 27mm |
| Rapid Development Kit | PCI 6140RDK | PCI 6150RDK | PCI 6152RDK | PCI 6152RDK | PCI 6154RDK | PCI 6254RDK | PCI 6466RDK | PCI 6520RDK | PCI 6540RDK |

* Available in standard and lead-free packaging. See complete list of part numbers on our website at http://www.plxtech.com/products/leadfree.asp

# FastLane™ PCI and PCI-X Bridges

## *Rapid Development Kits (RDKs)*

| | PCI 6140RDK | PCI 6152RDK | PCI 6150RDK | PCI 6154RDK | PCI 6254RDK | PCI 6466 RDK | PCI 6540RDK |
|---|---|---|---|---|---|---|---|
| Frequency on Primary | 33MHz | 33MHz | 25MHz - 66MHz | 25MHz - 66MHz | 25MHz - 66MHz | 33MHz - 66MHz | 33MHz - 133MHz |
| Frequency on Secondary | 33MHz | 33MHz | 25MHz - 66MHz | 25MHz - 66MHz | 25MHz - 66MHz | 33MHz - 66MHz | 33MHz - 133MHz |
| PCI rev compliance | r2.1 | r2.2 | r3.0 | r3.0 | r3.0 | r3.0 | r3.0 |
| Number of PCI slots on secondary | 5 | 4 | 4 | 5 | 5 | 4 | 4 |
| Asynchronous Mode | No | No | Yes | Yes | Yes | Yes | Yes |
| EEPROM | No | Yes | Yes | Yes | Yes | Yes | Yes |
| Optional BNC Connector/ Oscillator for secondary side | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Software support | Yes | Yes | Yes | Yes | Yes | Yes | Yes |



# *FastLane* PCI and PCI-X Bridges vs. Industry-Standards

| Standard Bridge | Bridge Type | Fast Lane Bridge Part Number | PKG-PINS | Fast Track Bridge® Advantages |
|---|---|---|---|---|
| 21150-BC | 32-bit / 66 MHz transparent | PCI 6150-BB66PC | PQFP-208 | • Asynchronous operation<br>• Performance-optimized retry<br>• EEPROM Support |
| GD21150-AC | 32-bit / 66 MHz transparent | PCI 6150-BB66BC | PBGA-256 | • Asynchronous operation<br>• Performance-optimized retry<br>• EEPROM Support |
| 21152-BB | 32-bit / 33 MHz transparent | PCI 6152-CC33PC | PQFP-160 | • 66MHz version available from PLX<br>• 15mm x 15mm Tiny BGA version available from PLX<br>• Lower power dissipation;<br>• Performance-optimized retry<br>• EEPROM Support |
| 21154-BE | 64-bit / 66 MHz transparent | PCI 6154-BB66BC | PBGA-304 | • Asynchronous operation<br>• Performance-optimized retry<br>• EEPROM Support<br>• 5V Tolerant I/O |
| 21554-AA* | 64-bit / 66 MHz transparent | PCI 6254-BB66BC | PBGA-365 | • Discontinued by original vendor; supported by PLX |
| 21555-BA* | 64-bit / 66 MHz non-transparent | PCI 6254-BB66BC | PBGA-365 | • PCI Rev. 3.0 Compliant |

* Functionally compatible

### PLX *FastLane* Bridges Advantages

- Better Performance than Common P-to-P Bridges
  - Large Buffer Sizes
  - Larger Prefetch Sizes
  - Smart Prefetch
  - Performance-Optimized Retry Architecture
  - Programmable Flow-Through
- Enhanced Compatibility
  - Asynchronous Clocking
  - Smaller Packages, Smaller Footprint BGA Versions
  - Lower Power Consumption
  - 5V Tolerant I/O
- Broad tools and customer service support

### *FastLane* Bridges Unique Features

- Non-Transparency
  - Benefit: Allows dual processor designs
  - Better performance, better data availability
- Universal Mode for CompactPCI
  - Allows a card to be system and peripheral card
  - Lowers inventory costs
- CompactPCI Hot-Swap Friendly
  - Simplifies hot swap designs
- EEPROM Support
  - Allows bridge configuration without driver support
- Smallest Packages
- Lowest Power Consumption

# PCI I/O Accelerators

PLX offers two types of I/O Accelerators: Targets (Table 1) and Masters (Table 2).

PCI Target I/O Accelerators support Direct Slave operation, PCI bus master devices to access memory and other slave devices on a local bus. They have broad application in adapters and embedded peripheral functions that are controlled from the PCI bus.

PCI Bus Master I/O Accelerators support Direct Slave operation, plus they add support for Direct Master operation, allowing processor/local bus master devices to access memory and other devices on the PCI bus, and they support DMA, allowing masters on either bus to direct the chip to perform data transfers. Mastering devices also provide intelligent messaging units for system control. They have broad application in intelligent peripheral devices and embedded hosts.

## Table 1. PCI Target I/O Accelerators

| Interfaces | PCI 9052 | PCI 9030-AA60PI<br>PCI 9030-AA60BI |
|---|---|---|
| PCI Bus Type | 32-bit, 33MHz PCI r2.1 | 32-bit, 33MHz PCI r2.2 |
| Local Bus Type(s) | C: Generic, 28-bit Address, 32-bit Data, non-muxed<br>J: Generic, 28-bit Address, 32-bit Data, muxed<br>I: ISA compatible | C: Generic, 28-bit Address, 32-bit Data, non-muxed<br>J: Generic, 28-bit Address, 32-bit Data, muxed |
| Maximum Local Bus Speed | 40MHz | 60MHz |
| Core Voltage | 5V | 3.3V |
| I/O Ring Voltage | 5V | 3.3V |
| 3.3V PCI and Local Bus | - | ✔ |
| 5V PCI and Local Bus | ✔ | ✔ (Tolerant) |
| PICMG 2.1 Hot Swap Support | - | r2.0 Hot Swap Silicon<br>Programming Interface 0 (PI=0)<br>Bias Voltage/Early Power |
| Package Size/Type(s) [pin/ball count, external dimensions (mm), pin/ball pitch (mm), package type] * | 160-pin, 31.2mm x 31.2mm, 0.65mm PQFP | 176-pin, 26mm x 26mm, 0.5mm PQFP<br>180-pin, 12mm x 12mm, 0.8mm µBGA |
| Industrial Temperature Range Operation | ✔ | ✔ |
| **Control** | | |
| PCI Power Management | - | ✔ (Revision 1.1) |
| PCI r2.2 VPD Support | - | ✔ |
| Serial EEPROM Support | 1-Kbit, 3-wire devices with sequential read support | 2-Kbit, 4-Kbit, 3-wire devices with sequential read support |
| JTAG Boundary Scan | - | ✔ |
| Register Compatibility | Backward compatible with PCI 9050 | Backward compatible with PCI 9050 |
| **Data Transfer** | | |
| Direct Slave Address Spaces | 4 General-Purpose 1 Expansion ROM | 4 General-Purpose 1 Expansion ROM |
| Direct Slave Read FIFO Depth | 8 Lwords (32 bytes) | 16 Lwords (64 bytes) |
| Direct Slave Write FIFO Depth | 16 Lwords (64 bytes) | 32 Lwords (128 bytes) |
| PCI r2.1 Deferred Read Support | ✔ | ✔ |
| Programmable READY# Time Out | - | ✔ |
| Programmable Pre-Fetch Counter | ✔ | ✔ |
| Big Endian/Little Endian Conversion | ✔ | ✔ |

Note: "-" means the product feature is not supported for that device.

* Available in standard and lead-free packaging. See complete list of part numbers on our website at http://www.plxtech.com/products/PCI9xxx_part_no.htm

# Table 2. PCI Bus Master I/O Accelerators

| Interfaces | PCI 9054-AC50PI<br>PCI 9054-AC50BI | PCI 9056-BA66BI | PCI 9656-BA66BI |
|---|---|---|---|
| PCI Bus Type | 32-bit, 33MHz PCI r2.2 | 32-bit, 66MHz PCI r2.2 | 64-bit, 66MHz PCI r2.2 |
| Local Bus Types(s) | C: Generic, 32-bit Address, 32-bit Data, non-muxed<br>J: Generic, 32-bit Address, 32-bit Data, muxed<br>M: PowerPC™ PowerQUICC™, 32-bit Address, 32-bit Data, non-muxed | C: Generic, 32-bit Address, 32-bit Data, non-muxed<br>J: Generic, 32-bit Address, 32-bit Data, muxed<br>M: PowerPC™ PowerQUICC™, 32-bit Address, 32-bit Data, non-muxed | C: Generic, 32-bit Address, 32-bit Data, non-muxed<br>J: Generic, 32-bit Address, 32-bit Data, muxed<br>M: PowerPC™ PowerQUICC™, 32-bit Address, 32-bit Data, non-muxed |
| Maximum Local Bus Speed | 50MHz | 66MHz | 66MHz |
| Core Voltage | 3.3V | 2.5V | 2.5V |
| I/O Ring Voltage | 3.3V | 3.3V | 3.3V |
| 3.3V PCI and Local Bus | ✔ | ✔ | ✔ |
| 5V PCI and Local Bus | ✔ (Tolerant) | ✔ (Tolerant) | ✔ (Tolerant) |
| PICMG 2.1 Hot Swap Support | r2.0 Hot Swap Silicon<br>Programming Interface 0 (PI=0) | r2.0 Hot Swap Silicon<br>Programming Interface 0 (PI=0)<br>Bias Voltage/Early Power Support<br>Initially Not Respond | r2.0 Hot Swap Silicon<br>Programming Interface 0 (PI=0)<br>Bias Voltage/Early Power Support<br>64-bit Initialization<br>Initially Not Respond |
| Package Size/Type(s) [pin/ball count, dimensions, pin/ball pitch, package type]* | 176-pin, 26mm x 26mm, .5mm PQFP<br>225-ball, 27mm x 27mm, 1.5mm PBGA | 256-ball, 17mm x 17mm, 1.0mm FPBGA | 272-ball, 27mm x 27mm, 1.27mm PBGA |
| Industrial Temperature Range Operation | ✔ | ✔ | ✔ |
| **Control** | | | |
| Mailbox Registers | Eight 32-bit | Eight 32-bit | Eight 32-bit |
| Doorbell Registers | Two 32-bit | Two 32-bit | Two 32-bit |
| I2O Messaging Unit | ✔ (Revision 1.5) | ✔ (Revision 1.5) | ✔ (Revision 1.5) |
| PCI Arbiter | - | ✔ (7 external masters) | ✔ (7 external masters) |
| PCI Type 0/1 Configuration Support | ✔ | ✔ | ✔ |
| PCI Power Management | ✔ (Revision 1.1) | ✔ (Revision 1.1) | ✔ (Revision 1.1) |
| D3COLD PME Generation | - | ✔ | ✔ |
| PCI r2.2 VPD Support | ✔ | ✔ | ✔ |
| Serial EEPROM Support | 2-Kbit, 4-Kbit, 3-wire devices with sequential read support | 2-Kbit, 4-Kbit, 3-wire devices with sequential read support | 2-Kbit, 4-Kbit, 3-wire devices with read support |
| JTAG Boundary Scan | - | ✔ | ✔ |
| Register Compatibility | Backward compatible with PCI 9080 | Backward compatible with PCI 9054 | Backward compatible with PCI 9054 |
| Direct Slave Address Spaces | 2 General-Purpose<br>1 Expansion ROM | 2 General-Purpose<br>1 Expansion ROM | 2 General-Purpose<br>1 Expansion ROM |

Note: "-" means the product feature is not supported for that device.

***** Available in standard and lead-free packaging. See complete list of part numbers on our website at http://www.plxtech.com/products/leadfree.asp

# Table 2. PCI Bus Master I/O Accelerators (continued)

| Data Transfer | PCI 9054-AC50PI<br>PCI 9054-AC50BI | PCI 9056-BA66BI | PCI 9656-BA66BI |
|---|---|---|---|
| Direct Slave Read FIFO Depth | 16 Lwords (64 bytes) | 32 Lwords (128 bytes) | 16 Qwords (128 bytes) |
| Direct Slave Write FIFO Depth | 32 Lwords (128 bytes) | 64 Lwords (256 bytes) | 32 Qwords (256 bytes) |
| PCI r2.1 Delayed Read Support | ✔ | ✔ | ✔ |
| Programmable READY# Time Out | - | ✔ | ✔ |
| Direct Master Address Spaces | 1 | 1 | 1 |
| Direct Master Read FIFO Depth | 16 Lwords (64 bytes) | 32 Lword (128 bytes) | 16 Qwords (128 bytes) |
| Direct Master Write FIFO Depth | 32 Lwords (128 bytes) | 64 Lwords (256 bytes) | 32 Qwords (256 bytes) |
| DMA Channels | 2 | 2 | 2 |
| DMA Channel 0 FIFO Depth | 32 Lwords (128 bytes)<br>Bi-directional | 64 Lwords (256 bytes)<br>Bi-directional | 32 Qwords (256 bytes)<br>Bi-directional |
| DMA Channel 1 FIFO Depth | 16 Lwords (64 bytes)<br>Bi-directional | 64 Lwords (256 bytes)<br>Bi-directional | 32 Qwords (256 bytes)<br>Bi-directional |
| DMA Demand Mode H/W Control | ✔ (Channel 0 Only) | ✔ | ✔ |
| DMA EOT Mode H/W Control | ✔ | ✔ | ✔ |
| DMA Block Mode | ✔ | ✔ | ✔ |
| DMA Scatter/Gather Mode | ✔ | ✔ | ✔ |
| DMA Ring Management Mode | - | ✔ | ✔ |
| Programmable Pre-Fetch Counter | ✔ | ✔ | ✔ |
| Dual Address Cycle Generation | ✔ | ✔ | ✔ |
| Big Endian/Little Endian Conversion | ✔ | ✔ | ✔ |

Note: "-" means the product feature is not supported for that device.

# PCI I/O Accelerator Rapid Development Kits

Rapid Development Kits (RDK) are comprehensive PCI development tool packages, which includes the PLX PCI HDK CD-ROM (see below), PCI SDK software CD-ROM, and a PCI or CompactPCI Reference Board.

| | PCI 9052 | PCI 9030 | | PCI 9054 | | PCI 9056 | | PCI 9656 | |
|---|---|---|---|---|---|---|---|---|---|
| **Part Number** | **PCI 9052 RDK-LITE** | **CompactPCI 9030RDK-LITE** | **PCI 9030 RDK-LITE** | **CompactPCI 9054RDK-860** | **PCI 9054 RDK-LITE** | **CompactPCI 9056RDK-860** | **PCI 9056 RDK-LITE** | **CompactPCI 9656RDK-860** | **PCI 9656 RDK-LITE** |
| PCI Compliance | PCI r2.1<br>32-bit, 33MHz | PICMG 2.0 r2.1<br>PICMG 2.1 r1.0<br>32-bit, 33MHz | PCI r2.2<br>32-bit, 33MHz | PICMG 2.0 r2.1<br>PICMG 2.1 r1.0 | PCI r2.2<br>32-bit, 33MHz | PICMG 2.0 r3.0<br>PICMG 2.1 r2.0<br>32-bit, 33MHz | PCI r2.2<br>32-bit, 66MHz | PICMG 2.0 r3.0<br>PICMG 2.1 r2.0<br>64-bit, 66MHz | PCI r2.2<br>64-bit, 66MHz |
| Local Bus | Non-muxed<br>28-bit Address<br>32-bit Data<br>40MHz<br>generic (C)<br>Configurable<br>to muxed (J) | Non-muxed<br>28-bit Address<br>32-bit Data<br>60MHz<br>generic (C)<br>Configurable<br>to muxed (J) | Non-muxed<br>28-bit Address<br>32-bit Data<br>60MHz<br>generic (C)<br>Configurable<br>to muxed (J) | 32-bit Address<br>32-bit Data<br>50MHz<br>PowerQUICC (M) | Non-muxed<br>32-bit Address<br>32-bit Data<br>50MHz<br>generic (C)<br>Configurable<br>to muxed (J) | 32-bit Address<br>32-bit Data<br>50MHz<br>PowerQUICC (M) | Non-muxed<br>32-bit Address<br>32-bit Data<br>66MHz<br>generic (C)<br>Configurable<br>to muxed (J) | 32-bit Address<br>32-bit Data<br>66MHz<br>PowerQUICC (M) | Non-muxed<br>32-bit Address<br>32-bit Data<br>66MHz<br>generic (C)<br>Configurable<br>to muxed (J) |
| CPU | - | User provided<br><br>Footprints<br>available<br>on board | User provided<br><br>Footprints<br>available<br>on board | Motorola<br>MPC860<br>PowerQUICC | User provided<br><br>Footprints<br>available<br>on board | Motorola<br><br>PowerQUICC | User provided<br>MPC860T<br>Footprints<br>available<br>on board | Motorola<br><br>PowerQUICC | User provided<br>MPC860T<br>Footprints<br>available<br>on board |
| SDRAM | - | - | - | 32 Mbytes<br>(8M x 32) | Footprints<br>available | 64 Mbytes<br>(16M x 32)<br>on Board | - | 64 Mbytes<br>(16M x 32) | - |
| SRAM | 128 Kbytes<br>(32K x 32) | 16 Kbytes<br>(8K x 16) | 16 Kbytes<br>(8K x 16) | 512 Kbytes<br>(128K x 32) | 128 Kbytes<br>(32K x 32) | 512 Kbytes<br>(128K x 32) | 512 Kbytes<br>(128K x 32) | 512 Kbytes<br>(128K x 32) | 128 Kbytes<br>(32K x 32) |
| Boot ROM Flash | Socket<br>available<br>on board | Socket<br>available<br>on board | Socket<br>available<br>on board | 512 Kbytes<br>(512K x 8) | Socket<br>available<br>on board | 512 Kbytes<br>(512K x 8) plus<br>8Mbytes (8M x 8) | Socket<br>available<br>on board | 512 Kbytes<br>(512K x 8) plus<br>8Mbytes (8M x 8) | Socket<br>available<br>on board |
| Communication Port(s) | - | RS-232 Serial | RS-232 Serial | RS-232 Serial | RS-232 Serial | RS-232 Serial (2),<br>10/100 Mbit | RS-232 Serial<br><br>Ethernet | RS-232 Serial (2),<br>10/100 Mbit | RS-232 Serial<br><br>Ethernet |
| Debug Port(s) Software Included | -<br>PCI SDK | -<br>PCI SDK | -<br>PCI SDK | BDM<br>PCI SDK | PCI SDK | BDM<br>PCI SDK | -<br>PCI SDK | BDM<br>PCI SDK | -<br>PCI SDK |
| PLX Option Module (POM) Connector | - | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |

Note: "-" means the product feature is not supported for that device.

## Hardware Development Kit CD-ROM Collection

The PCI Hardware Development Kit (HDK) CD-ROM Collection is a comprehensive assortment of PLX hardware tools. It includes the contents of the above product HDKs on a single CD-ROM, plus all current Application Notes and the OrCAD Capture Symbol Library. It contains complete hardware design information including OrCAD Schematics, Gerber Layout Files, OrCAD layout source files, Bill of Materials (BOM), Hardware Reference Manuals, Verilog source code (where applicable), PLX chip Data Books, and Product Briefs.

# PCI Software Development Kit (SDK)

PLX's PCI SDK 4.4 is an invaluable tool for PCI software developers. The following table details its extensive software components. The PCI SDK 4.4 CD-ROM also contains complete documentation including the PCI SDK User's Manual and PCI SDK Programmer's Reference Manual.

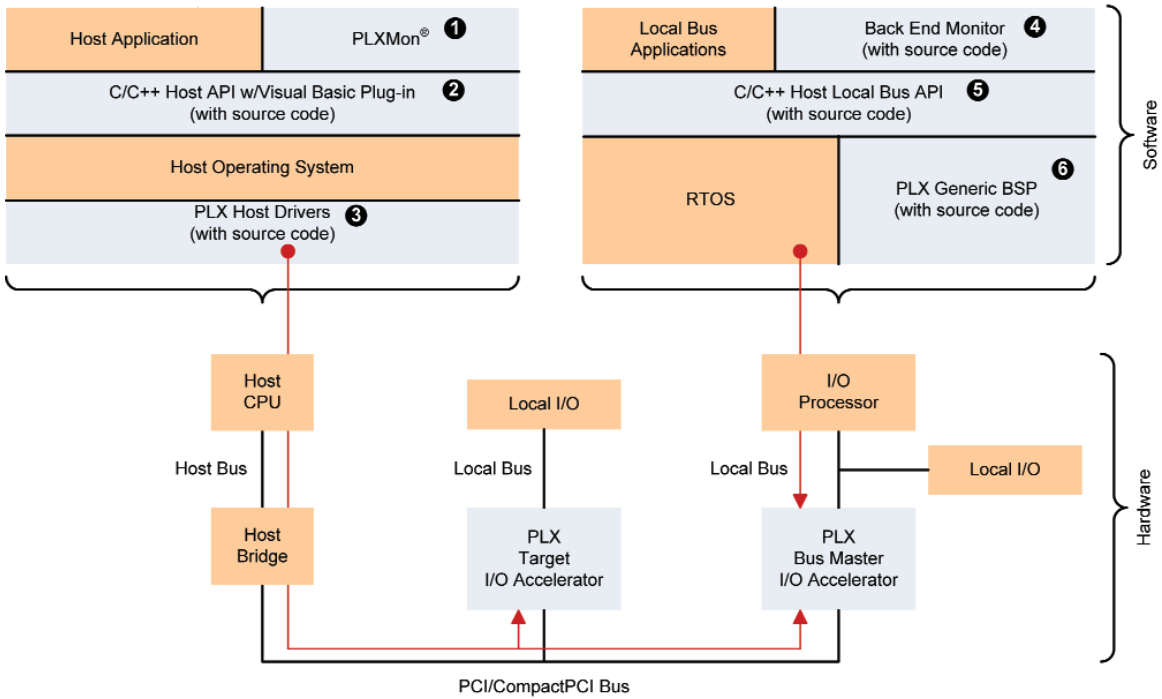
**Supported Chips and Rapid Development Kits**

| SDK 4.4 Software Component | | PEX 8311 | PCI 9030 | PCI 9030RDK-LITE | CompactPCI 9030RDK-LITE | PCI 9052 | PCI 9052RDK-LITE | PCI 9054 | PCI 9054RDK-LITE | CompactPCI 9054RDK-860 | PCI 9056 | PCI 9056RDK-LITE | CompactPCI 9056RDK-860 | PCI 9080 | PCI 9656 | PCI 9656RDK-LITE | CompactPCI 9656RDK-860 | PCI 6140 + RDK | PCI 6150 + RDK | PCI 6152 + RDK | PCI 6154 + RDK | PCI 6156 + RDK | PCI 6254 + RDK | PCI 6466 + RDK | PCI 6520 | PCI 6540 + RDK |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Windows Applications** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PLXMon™ Support Interactive Windows-Based GUI | 1 | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| PLXMon Performance Measure | 1 | ✔ | ✔ | | | ✔ | | ✔ | | | ✔ | | | ✔ | ✔ | | | * | * | * | * | * | * | * | * | * |
| **PCI Software Development Support** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C/C++ API Library Object & Source Files | 2 | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| Source code Using PCI API library, Non-transparent mode, etc. | 2 | ✔ | | | | | | | | | | | | | | | | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| Source Code Examples Using PCI API Library Direct Slave Transfer, Interrupt Event Handling, Scatter/Gather DMA, and more | 2 | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | | | | | |
| MS Windows (32-bit & 64-bit(x64)) Host Drivers with Source Code | 3 | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| Linux Kernel 2.4 & 2.6 (32-bit & 64-bit) Host Drivers with Source Code | 3 | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | | | | | |
| **Local Bus Software Development Support** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Back-End Monitor Executable & Source Code Enables Local Bus Communication With PCI Application via the RDK Serial Port | 4 | ✔ | | | | | | ✔ | | ✔ | ✔ | | ✔ | | ✔ | | ✔ | | | | | | | | | |
| Source Code Examples Using Local Bus API Library Direct Master Transfer, Block Mode DMA, & Scatter/Gather DMA, and more | 5 | ✔ | | | | | | ✔ | | ✔ | ✔ | | ✔ | | ✔ | | ✔ | | | | | | | | | |
| C/C++ API Library Object Files & Source Code Create Local Bus Executables | 5 | ✔ | | | | | | ✔ | | ✔ | ✔ | | ✔ | | ✔ | | ✔ | | | | | | | | | |
| PLX Board Support Package (BSP) Executable & Source Code Generic Local Bus Software Environment | 6 | ✔ | | | | | | ✔ | | ✔ | ✔ | | ✔ | | ✔ | | ✔ | | | | | | | | | |

*PLX Performance Measure Tool can be used to estimate performance on the PCI 6000 series in conjunction with the PCI 9056RDK-860 and CompactPCI 9656RDK-860 DMA boards.

The figure below illustrates the PCI SDK architecture: the types of software components included, how these components interface with each other, and how they interface with a system that includes one or more PLX PCI I/O Accelerators.

## PCI SDK Block Diagram





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